WHAT IS CLAIMED IS:

1. An integrated circuit comprising a memory array including memory cells arranged in a plurality of series-connected NAND strings, said memory cells comprising modifiable conductance switch devices, said NAND strings including at a first end thereof a respective plurality of series selection devices.

2. The integrated circuit as recited in claim 1 wherein the memory array comprises a two-dimensional memory array having one plane of memory cells formed in a substrate.

3. The integrated circuit as recited in claim 1 wherein the memory array comprises a three-dimensional memory array having at least two planes of memory cells formed above a substrate.

4. The integrated circuit as recited in claim 3 wherein the substrate comprises a monocrystalline substrate including circuitry which is coupled to the memory array.

5. The integrated circuit as recited in claim 3 wherein the substrate comprises a polycrystalline substrate.

6. The integrated circuit as recited in claim 3 wherein the substrate comprises an insulating substrate.

7. The integrated circuit as recited in claim 1 wherein the modifiable conductance switch devices comprise transistors having a depletion mode threshold voltage at least some of the time.

8. The integrated circuit as recited in claim 1 wherein the modifiable conductance switch devices comprise transistors having a respective threshold voltage which is modifiable post-manufacture.

9. The integrated circuit as recited in claim 8 wherein the modifiable conductance switch devices comprise a floating gate electrode.

10. The integrated circuit as recited in claim 8 wherein the modifiable conductance switch devices comprise silicon nanoparticles.

11. The integrated circuit as recited in claim 8 wherein the modifiable conductance switch devices comprise a polarizable material.

12. The integrated circuit as recited in claim 8 wherein the modifiable conductance switch devices comprise a ferroelectric material.

13. The integrated circuit as recited in claim 1 wherein the modifiable conductance switch devices comprise thin film transistor (TFT) devices.

14. The integrated circuit as recited in claim 8 wherein the modifiable conductance switch devices comprise transistors having a charge storage dielectric.

15. The integrated circuit as recited in claim 14 wherein the charge storage dielectric comprises an oxide-nitride-oxide (ONO) stack.

16. The integrated circuit as recited in claim 14 wherein the memory cell transistors have a depletion mode threshold voltage when the charge storage dielectric has a minimum stored negative charge level.

17. The integrated circuit as recited in claim 14 wherein the memory cell transistors have a depletion mode threshold voltage when the charge storage dielectric has a minimum stored positive charge level.

18. The integrated circuit as recited in claim 14 wherein the memory cell transistors have a first depletion mode threshold voltage corresponding to an erased data state and have a second depletion mode threshold voltage corresponding to a programmed data state.

19. The integrated circuit as recited in claim 1 wherein the memory cell switch devices have more than two nominal values of conductance, for storing more than one bit of data per memory cell.

20. The integrated circuit as recited in claim 1 wherein the selection devices and memory cell devices forming each NAND string are structurally substantially identical.

21. The integrated circuit as recited in claim 1 wherein each NAND string includes at least one series selection device at a second end thereof opposite the first end.

22. The integrated circuit as recited in claim 1 wherein respective select signals corresponding to at least two respective ones of the first plurality of series selection devices for a selected NAND string are driven to different levels during at least one memory operation.

23. The integrated circuit as recited in claim 22 wherein, during a programming operation for a selected NAND string, the respective select signal corresponding to one of the first plurality of series selection devices is driven to ground, and the respective select signal corresponding to another one of the first plurality of series selection devices is driven to a voltage between ground and a programming voltage conveyed on a selected word line.

24. The integrated circuit as recited in claim 21 wherein pairs of NAND strings are arranged so that:

the respective second end of each string of the pair is coupled to a respective global array line; and

the respective first end of each string of the pair is coupled to a shared bias node.

25. The integrated circuit as recited in claim 21 wherein each NAND string includes a second plurality of series selection devices at the second end thereof.

26. The integrated circuit as recited in claim 25 wherein pairs of NAND strings are arranged so that:

a first group of control signals couples the respective second end of one string of the pair to a global array line associated with the pair, and couples

the respective first end of the other string of the pair to a respective bias node; and

a second group of control signals couples the respective first end of said one string of the pair to a respective bias node, and couples the respective second end of the other string of the pair to the global array line associated with the pair.

27. The integrated circuit as recited in claim 21 comprising series selection devices having a charge storage dielectric.

28. The integrated circuit as recited in claim 27 comprising series selection devices which are maintained by periodic programming biasing to a higher threshold voltage than fabricated.

29. The integrated circuit as recited in claim 3 wherein NAND strings on more than one memory level are respectively coupled to global array lines disposed on fewer levels than said more than one memory level.

30. The integrated circuit as recited in claim 3 wherein a respective plurality of NAND strings on each of at least two memory levels are coupled to a single global array line disposed on a single level of the integrated circuit.

31. The integrated circuit as recited in claim 3 wherein the modifiable conductance switch devices comprise thin film transistor (TFT) devices having a charge storage dielectric.

32. The integrated circuit as recited in claim 31 wherein the memory cell transistors have a depletion mode threshold voltage when the charge storage dielectric has a minimum stored negative charge level.

33. The integrated circuit as recited in claim 31 wherein:

each NAND string includes at least one series selection device at a second end thereof opposite the first end; and

the series selection devices and memory cell devices forming each NAND string are structurally substantially identical.

34. The integrated circuit as recited in claim 33 wherein, during a programming operation, a respective select signal corresponding to one of the first plurality of series selection devices is driven to ground, and a respective select signal corresponding to another one of the first plurality of series selection devices is driven to a voltage between ground and a programming voltage conveyed on a selected word line.

35. The integrated circuit as recited in claim 34 wherein pairs of NAND strings are arranged so that:

a first group of at least one control signal couples the respective second end of each string of the pair to a respective global array line; and

a second group of control signals couples the respective first end of each string of the pair to a shared bias node.

36. The integrated circuit as recited in claim 35 wherein, during a programming operation, the shared bias node is driven to a voltage between ground and a bit line inhibit voltage conveyed to an unselected NAND string sharing word lines with the selected NAND string.

37. The integrated circuit as recited in claim 36 wherein, during a programming operation, more than one NAND string is selected in a selected block of the memory array.

38. The integrated circuit as recited in claim 1 embodied in computer readable descriptive form suitable for use in design, test or fabrication of said integrated circuit.

39. An integrated circuit including a memory array arranged in a plurality of blocks, said integrated circuit comprising:

a first memory block comprising

a first bias node;

a plurality of global bit lines traversing across the first block in a first direction;

a plurality of word lines traversing across the first block in a second direction different than the first direction;

a first group of one or more select lines traversing across the first block generally parallel to and disposed on one side of the plurality of word lines;

a second group of more than one select lines traversing across the first block generally parallel to and disposed on the other side of the plurality of word lines; and

a plurality of series-connected NAND strings, each comprising, at a first end thereof, a first group of one or more series select devices each responsive to a respective one of the first group of one or more select lines, further comprising a plurality of memory cell devices each responsive to a respective one of the plurality of word lines, and further comprising, at a second end thereof, a second group of more than one block select devices each responsive to a respective one of the second group of more than one select lines.

40. The integrated circuit as recited in claim 39 wherein:

the first end of each NAND string is respectively coupled to a respective one of the plurality of global bit lines; and

the second end of each NAND string is respectively coupled to the first bias node.

41. The integrated circuit of claim 40 comprising global bit lines disposed on more than one global bit line layer.

42. The integrated circuit of claim 41 comprising even-numbered global bit lines disposed on a first global bit line layer and odd-numbered global bit lines disposed on a second global bit line layer.

43. The integrated circuit of claim 40 wherein global bit lines respectively associated with each of a pair of adjacent NAND strings are disposed on different layers of the integrated circuit.

44. The integrated circuit as recited in claim 39:

wherein the first memory block further comprises a second bias node;

wherein the first end of each of a first group of the NAND strings is respectively coupled to a corresponding one of the plurality of global bit lines, and the first end of each of a second group of the NAND strings is respectively coupled to the first bias node; and

wherein the second end of each of the first group of the NAND strings is respectively coupled to the second bias node, and the second end of each of the second group of the NAND strings is respectively coupled to a corresponding one of the plurality of global bit lines.

45. The integrated circuit as recited in claim 39 wherein:

pairs of NAND strings are coupled to the same global bit line, each such pair including a NAND string from each of the first and second groups of NAND strings, thereby providing for a global bit line pitch which is half that of the NAND strings.

46. The integrated circuit as recited in claim 39 wherein:

more than one physically adjacent NAND strings of the first memory block share a contact to the first or second bias nodes.

47. The integrated circuit as recited in claim 39 wherein:

each NAND string of the first memory block contacts its associated global bit line by way of a via which is shared by a corresponding NAND string of another memory block having different word lines.

48. The integrated circuit as recited in claim 39 wherein:

each NAND string of the first memory block contacts its associated global bit line by way of a via which is shared by a corresponding NAND string of another memory block disposed on another memory plane.

49. The integrated circuit as recited in claim 39 wherein:

each of the first group of NAND strings of the first memory block contacts its associated global bit line by way of a via which is shared by a NAND string of another memory block on the same memory plane as the first memory block.

50. The integrated circuit as recited in claim 39 wherein:

the memory cell devices comprise transistors having a charge storage dielectric.

51. The integrated circuit as recited in claim 39 wherein:

the memory cell devices comprise transistors having a respective threshold voltage which is modifiable post-manufacture.

52. The integrated circuit as recited in claim 39 wherein:

the first and second plurality of block select devices of a given NAND string are structurally identical to the memory cell transistors of the given NAND string.

53. The integrated circuit as recited in claim 39 wherein:

the memory cell transistors of a given NAND string have a depletion mode threshold voltage for at least one of two data states.

54. The integrated circuit as recited in claim 1 embodied in computer readable descriptive form suitable for use in design, test or fabrication of said integrated circuit.

55. A method for programming a memory cell in a memory array, said memory array having at least one plane of memory cells, said memory cells comprising modifiable conductance switch devices arranged in a plurality of series-connected NAND strings, said method comprising:

selecting a block of the array, a NAND string within the selected block, and a memory cell within the selected NAND string;

coupling a first end of the selected NAND string to a selected global bit line by turning on each of a group of one or more series select devices at the first end of the selected NAND string;

de-coupling a second end of the selected NAND string from a first shared bias node by turning off at least one of a plurality of series select devices at the second end of the selected NAND string;

impressing a bit line programming voltage onto the selected global bit line to program the selected memory cell or a bit line inhibit voltage to inhibit programming of the selected memory cell; and

pulsing the selected word line to a word line programming voltage, to conditionally program the selected memory cell in accordance with the voltage impressed on the selected global bit line.

56. The method as recited in claim 55 further comprising:

coupling a first end of an unselected NAND string in the selected block to an unselected global bit line, said second NAND string having word lines in common with the selected NAND string; and

impressing a bit line inhibit voltage onto the unselected global bit line to inhibit programming of memory cells in the unselected NAND string;

57. The method as recited in claim 55 further comprising:

coupling a first end of an unselected NAND string in the selected block to a second bias line, said second NAND string having word lines in common with the selected NAND string;

de-coupling a second end of the unselected NAND string from an associated global bit line by turning off at least one of a plurality of series select devices at the second end of the unselected NAND string; and

impressing a bias inhibit voltage onto the second bias line to inhibit programming of memory cells in the unselected NAND string;

58. The method as recited in claim 55 wherein:

the inhibit bias voltage is substantially the same as the bit line inhibit voltage.

59. The method as recited in claim 55 wherein:
the modifiable conductance switch devices comprise transistors having a charge storage dielectric.

60. The method as recited in claim 55 wherein:
the modifiable conductance switch devices comprise transistors having a respective threshold voltage which is modifiable post-manufacture.